AD - Converter

ICL7136

Single Chip AD – Converter

DATASHEET

OEM – Intersil

Source: Intersil Databook 1987

Datasheet Rev. 1.0 – 10/20 – data without warranty / liability

ICL7137

ICL7137
3½-Digit LED Low Power Single-Chip A/D Converter

GENERAL DESCRIPTION

The Intersil ICL7137 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7137 is designed to interface with a light emitting diode (LED) display. The supply current (exclusive of display) is under 200μA, ideally suited for battery operation.

The 7137 brings together an unprecedented combination of high accuracy, versatility, and true economy. The device features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of the ICL7137 allows a high performance panel meter to be built with the addition of only 10 passive components and a display.

The ICL7137 is an improved version of the ICL7107, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications, changing only the passive component values.

FEATURES

- **First-Reading Recovery From Overrange allows Immediate "OHMS" Measurement**
- **Guaranteed Zero Reading for 0V Input**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Typical Input Current**
- **True Differential Input and Reference**
- **Direct LED Display Drive — No External Components Required**
- **Pin Compatible With The ICL7107**
- **Low Noise — 15μVp-p Without Hysteresis or Overrange Hangover**
- **On-Chip Clock and Reference**
- **Improved Rejection of Voltage On COMMON Pin**
- **No Additional Active Circuits Required**
- **Evaluation Kit Available ICL7137EV/Kit**

ORDERING INFORMATION*

Part Number	Temperature Range	Package
ICL7137CPL	0°C to +70°C	40-Pin Plastic
ICL7137RCPL	0°C to +70°C	40-Pin Plastic
ICL7137EV/KIT		EVALUATION KIT

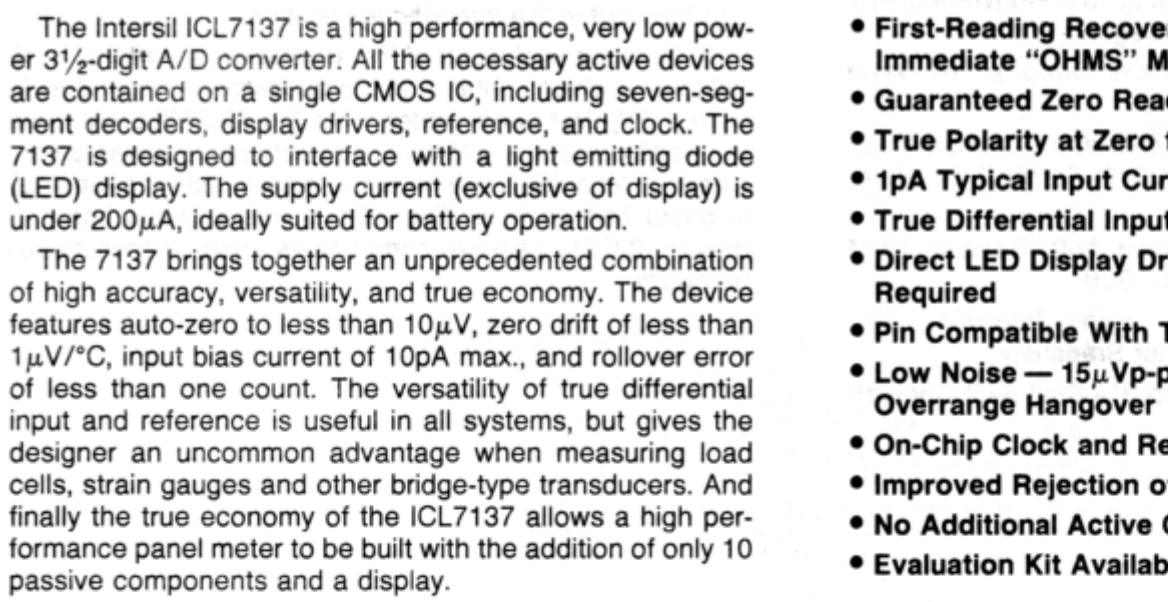

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Figure 1: Functional Diagram

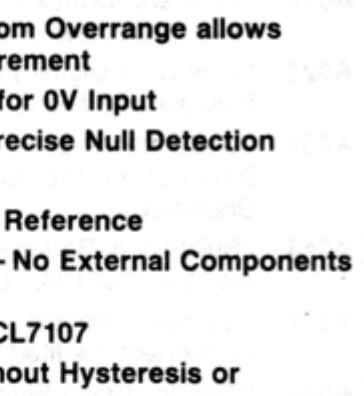

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Figure 2: Pin Configuration*

(Outline dwgs PL, JL, DL)

301669-002

NOTE: All typical values have been characterized but are not tested.

ICL7137

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (Note 3)

Parameter	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	998	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \cong$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		30		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. Oppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not Include LED current)	V_{IN} = 0V (Note 5)		70	200	μA
V^- Supply current			40		
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		150		ppm/°C
Segment Sinking Current (Except Pins 19 & 20) (Pin 19 only) (Pin 20 only)	V^+ = 5.0V Segment Voltage = 3V	5 10 4	8.0 16 7		mA
Power Dissipation Capacitance	vs. Clock Frequency		40		pF

NOTES: **3.** Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 4.
4. Refer to "Differential Input" discussion.
5. 48kHz oscillator, Figure 5, increases current by 35μA (typ).
6. Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

NOTE: All typical values have been characterized but are not tested.

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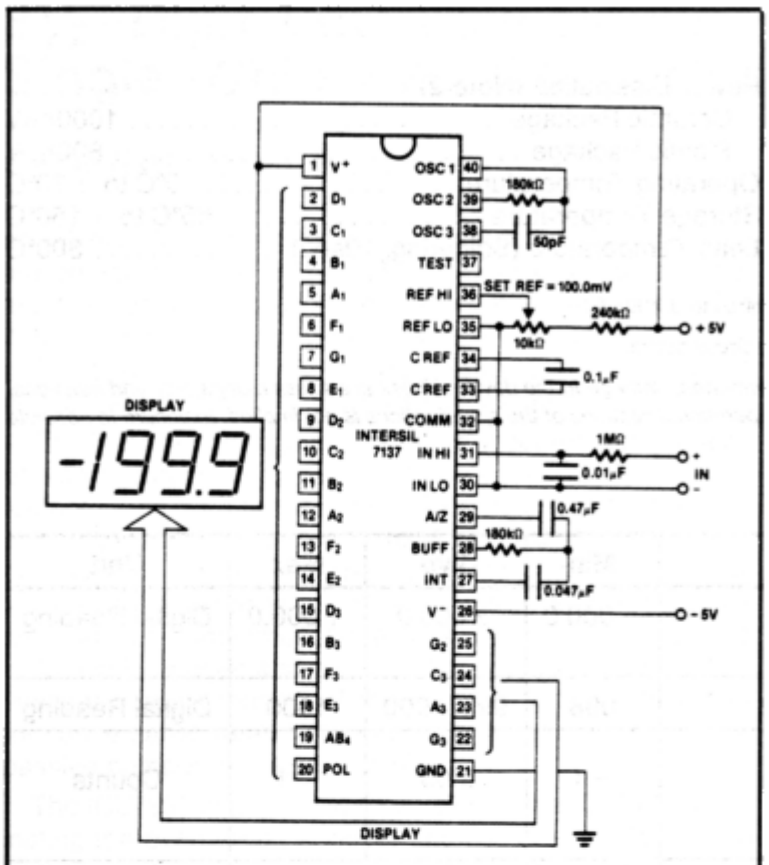

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Figure 3: ICL7137 with LED Display

TEST CIRCUITS

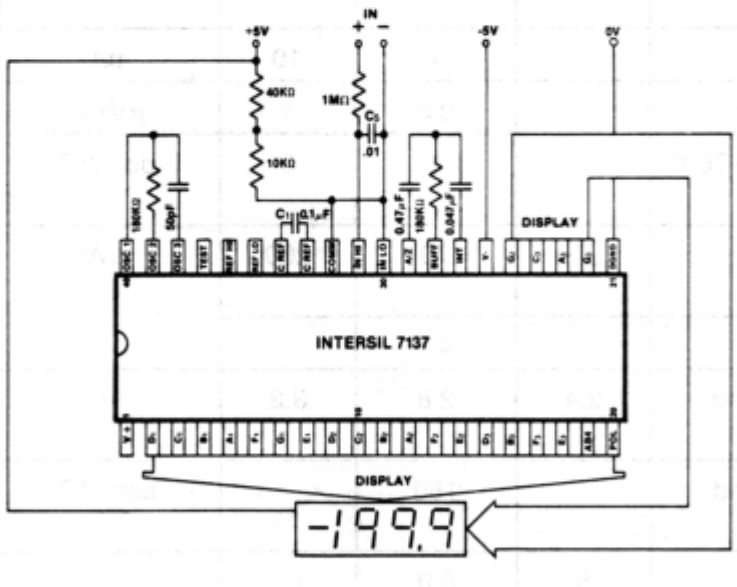

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Figure 4: 7137 Clock Frequency 16kHz (1 reading/sec)

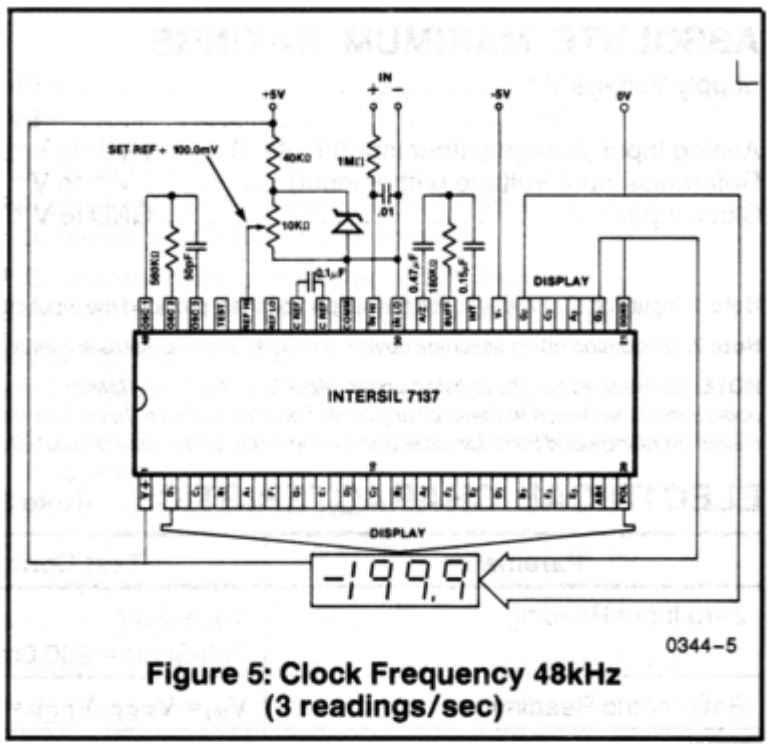

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Figure 5: Clock Frequency 48kHz (3 readings/sec)

DETAILED DESCRIPTION (Analog Section)

Figure 1 shows the Functional Diagram of the Analog Section for the ICL7137. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero-integrator (ZI).

AUTO-ZERO PHASE

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

NOTE: All typical values have been characterized but are not tested.

DE-INTEGRATE PHASE

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically; the digital reading displayed is $1000(V_{IN}/V_{REF})$.

ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 90dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Value Selection).

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance(≅35Ω), and a temperature coefficient typically less than 150ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2°C to 8°C, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Figure 6.

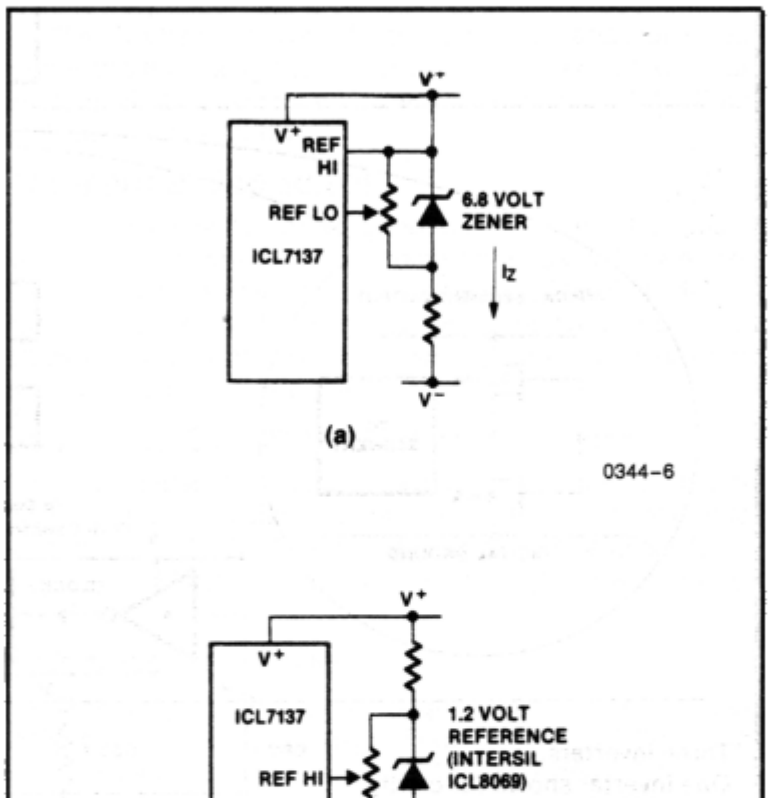

Figure 6: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

NOTE: All typical values have been characterized but are not tested.

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Within the IC, analog COMMON is tied to an N channel FET which can sink 100μA or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

TEST

The TEST pin is coupled to the internal digital supply through a 500Ω resistor, and functions as a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

DISPLAY FONT

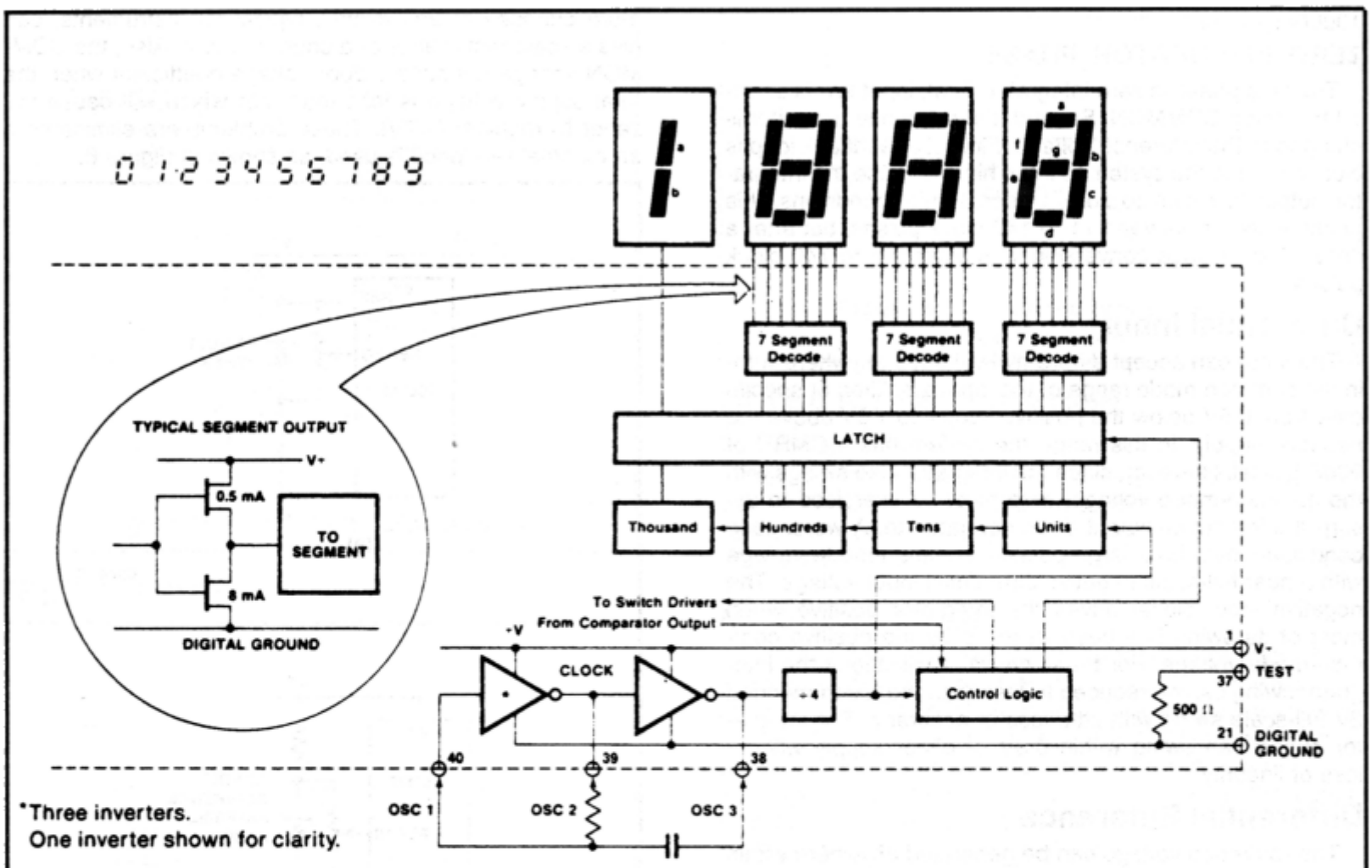

Figure 7: Digital Section

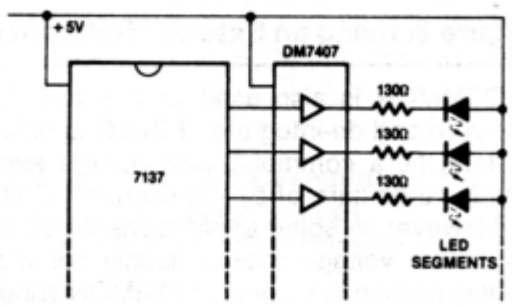

Figure 8: Display Buffering for Increased Drive Current

DETAILED DESCRIPTION (Digital Section)

Figure 7 shows the digital section for the 7137. The segments are driven at 8mA, suitable for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

Figure 8 shows a method of increasing the output drive current, using four DM7407 Hex Buffers. Each buffer is capable of sinking 40mA.

NOTE: All typical values have been characterized but are not tested.

System Timing

Figure 9 shows the clock oscillator provided in the 7137. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

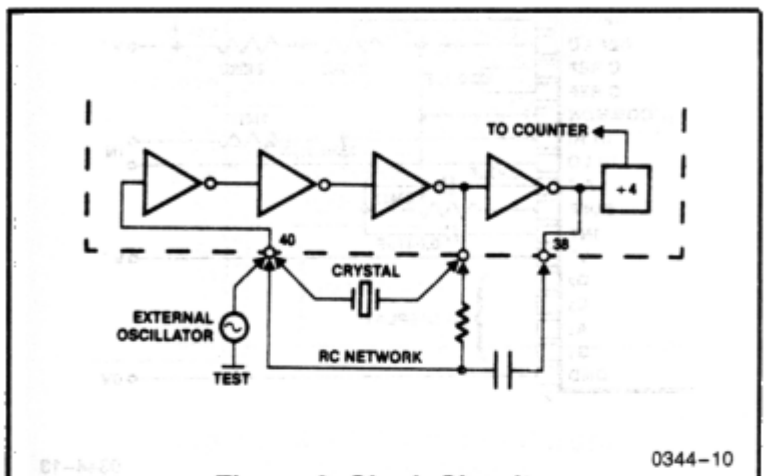

Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts), zero integrator (11 counts to 140 counts*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33⅓kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66⅔kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz.) See also A052.

*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

COMPONENT VALUE SELECTION

(See Application Note A052)

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 1.8MΩ is near optimum, and similarly 180kΩ for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal ±2V full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1 reading/second (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47μF capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7107 or ICL7117 (See Application Note A032).

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally, 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \cong 0.45/RC$. For 48kHz clock (3 readings/second), R = 180kΩ, while for 16kHz (1 reading/sec), R = 560kΩ.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2,000V scale, V_{REF} should equal 100.0mV and 1.000V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. A suitable value for the integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

The 7137 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

NOTE: All typical values have been characterized but are not tested.

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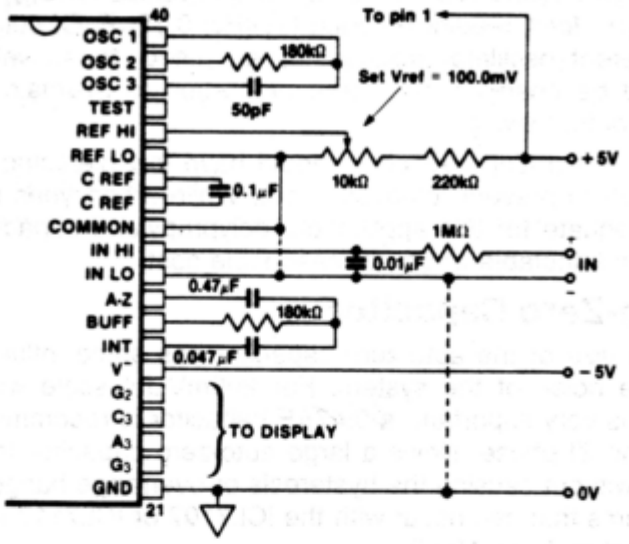

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Figure 10: 7137 Using the Internal Reference.

Values shown are for 200.0mV full-scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

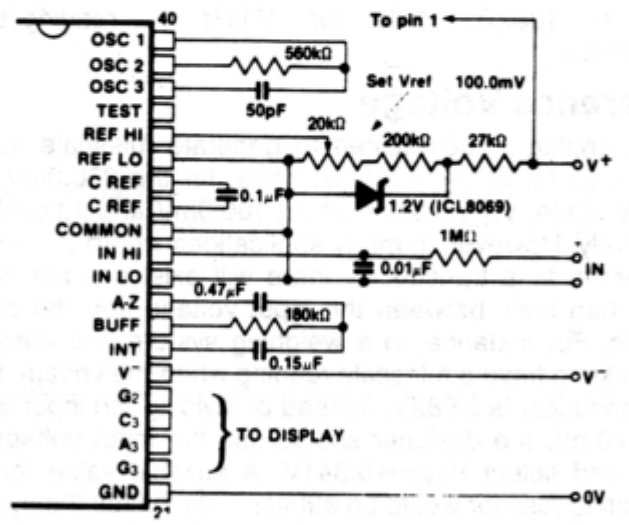

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Figure 11: 7137 with an External Band-Gap Reference (1.2V Type).

IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.

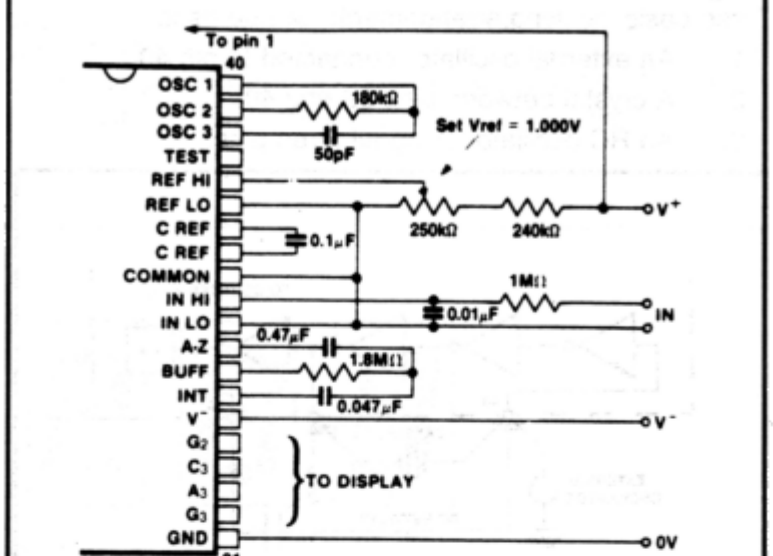

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Figure 12: Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec.

For 1 reading/sec, change C_{INT}, R_{OSC} to values of Figure 11.

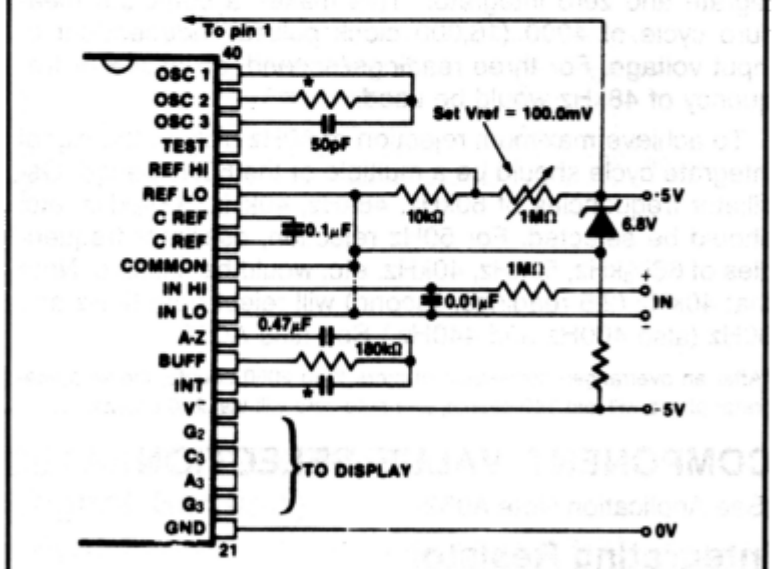

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Figure 13: 7137 with Zener Diode Reference.

Since low TC zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 11, IN LO may be tied to COMMON.

NOTE: All typical values have been characterized but are not tested.

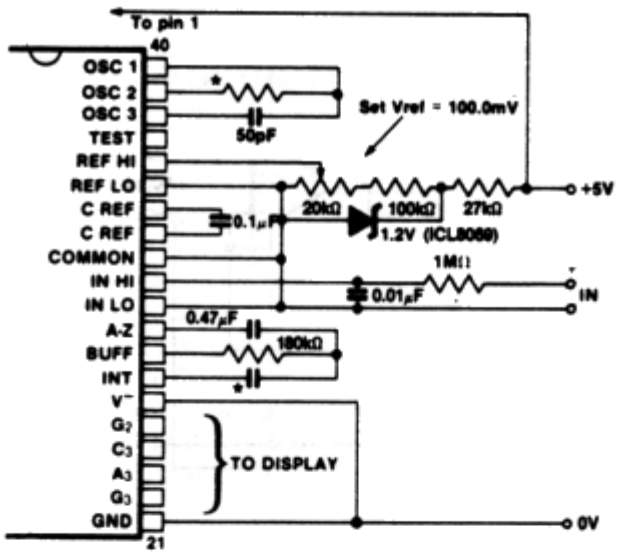

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Figure 14: 7137 Operated from Single +5V Supply.

An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

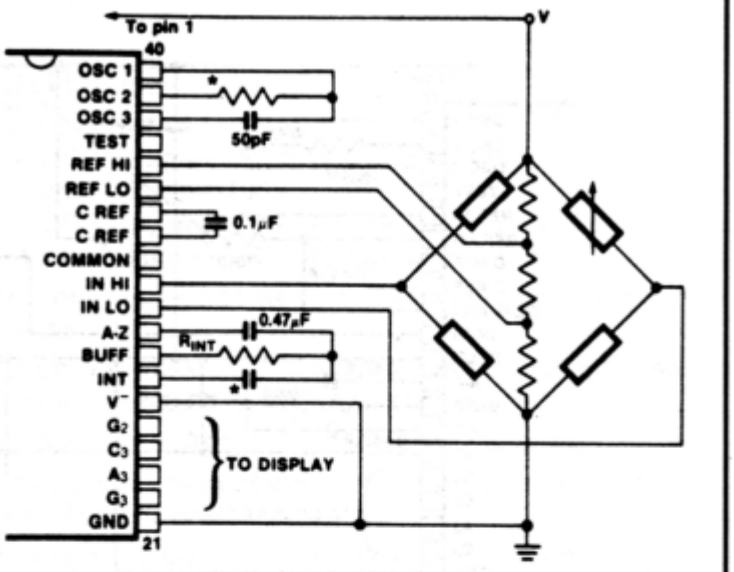

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Figure 15: Measuring Ratiometric Values of Quad Load Cell.

The resistor values within the bridge are determined by the desired sensitivity.

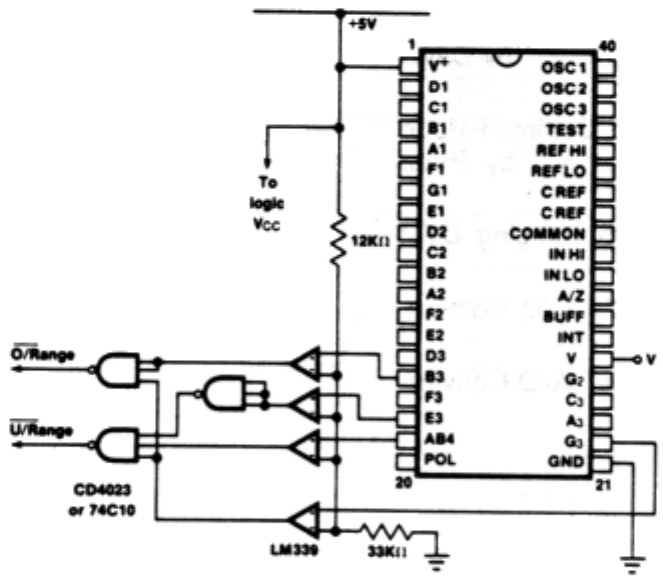

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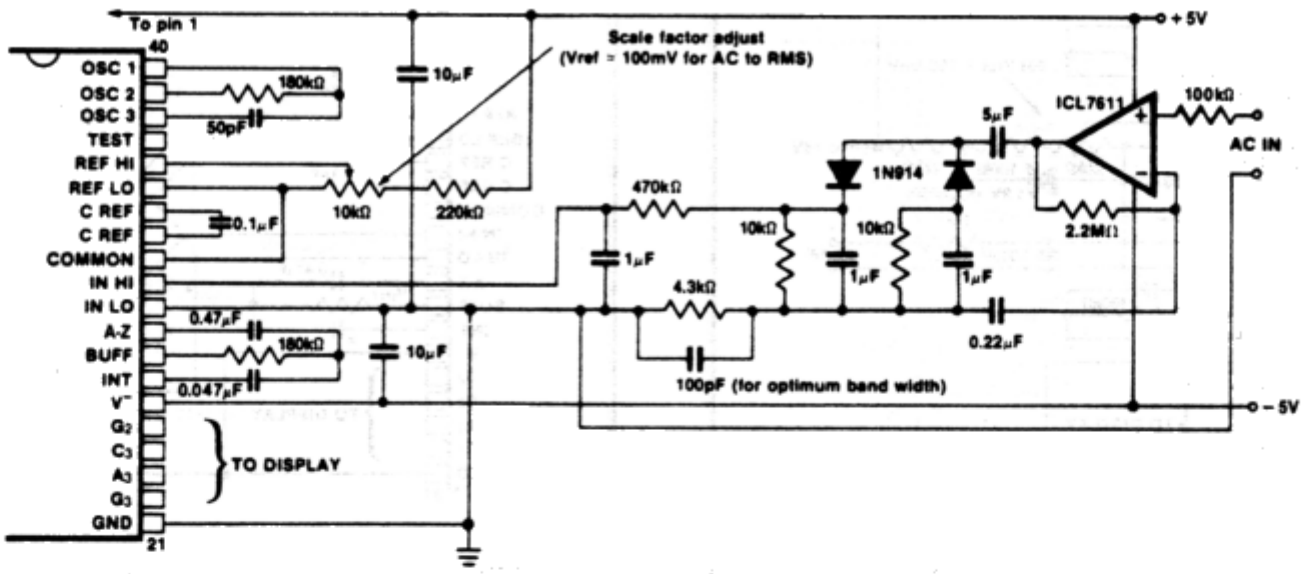
Figure 16: Circuit for developing Underrange and Overrange signals from outputs.

The LM339 is required to ensure logic compatibility with heavy display loading.

*Values depend on clock frequency. See Figures 10, 11, and 12.

NOTE: All typical values have been characterized but are not tested.



0344-18

Figure 17: AC to DC Converter with 7137

APPLICATION NOTES

A016 "Selecting A/D converters," by David Fullagar.

A017 "The Integrating A/D Converter," by Lee Evans.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.

A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.

A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.

A047 "Games People Play with Intersil's A/D Converters" edited by Peter Bradshaw.

A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

ICL7137 EVALUATION KITS

After purchasing a sample of the 7137, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7137EV/Kit, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, LED display, passive components, and miscellaneous hardware.

NOTE: All typical values have been characterized but are not tested.